

MuYu

MY-BT302D

Bluetooth 5.2 Audio + Data Module
Version 1.0

Contact Us

Shenzhen Muyu Technology Co., Ltd

Email: info@muyusmart.com

Zipcode: 518100

Web: www.muyumodule.com



Release Recode

Version	Date	Comments
1.0	2020/06/01	Initial Version

Shenzhen Muyu Technology Co., Ltd

Content

1	INTRODUCTION	4
1.1	Overview.....	4
1.2	Features.....	4
1.3	Application.....	6
2	GENERAL SPECIFICATION	6
2.1	Audio performance	7
3	HARDWARE SPECIFICATION	10
3.1	Block Diagram and Pin Definition Diagram	10
3.2	PIN Definition Descriptions	11
4	PHYSICAL INTERFACE	13
4.1	UART interface	13
4.2	SPI master.....	14
4.3	I ² C master	15
5	ELECTRICAL CHARACTERISTICS.....	15
5.1	Battery input pin specification.....	15
5.2	Charger input pin specification.....	16
5.3	Digital terminals	16
5.4	LED driver pads.....	17
5.5	VBAT voltage measurement accuracy	17
5.6	Absolute Maximum Ratings	17
5.7	Recommended Operating Conditions.....	17
6	ESD & MSL.....	17
7	RECOMMENDED TEMPERATURE REFLOW PROFILE.....	18
8	MECHANICAL DETAIL	19
8.1	Physical Dimensions	19
9	HARDWARE INTEGRATION SUGGESTIONS.....	20
9.1	Soldering Recommendations.....	20
9.2	Layout Guidelines (Internal Antenna).....	20
9.3	Layout Guidelines (External Antenna)	21
9.4	General Design Suggestions	22
10	PRODUCT PACKAGING INFORMATION	22
11	APPLICATION SCHEMATIC	23

1 Introduction

1.1 Overview

MY-BT302 Bluetooth Module is a high performance, cost effective, low power and compact solution. The Bluetooth module provides highest level of integration with integrated 2.4GHz radio, DSP, Power management, battery Charger, stereo audio Codec based on the QCC3040 BGA chipset. It can be designed for mono and stereo audio applications. This module supports Bluetooth v5.2 BR/EDR and BLE Dual mode standard.

1.2 Features

- Qualified to Bluetooth v5.2 specification
- 120 MHz Qualcomm® Kalimba™ audio DSP
- 32 MHz Developer Processor for applications
- Firmware Processor for system
- Flexible QSPI flash programmable platform
- High-performance 24- bit audio interface
- Digital and analog microphone interfaces
- Flexible PIO controller and LED pins with PWM support
- Serial interfaces: UART, Bit Serializer (I²C/SPI), USB 2.0
- Advanced audio algorithms
- Active Noise Cancellation: Hybrid, Feedforward, and Feedback modes, using Digital or Analog Mics, enabled using license keys available from Qualcomm®
- Qualcomm® aptX™ and aptX HD Audio
- 1 or 2 mic Qualcomm® cVc™ headset speech processing
- Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger
- **Audio subsystem**
- 32- bit Kalimba audio digital signal processor (DSP) core with flexible clocking from 2 MHz to 120 MHz to enable optimization of performance vs. power consumption
- DSP executes code from ROM
- 112 KB program random access memory (RAM)
- 448 KB data RAM
- 6 Mb ROM
- **Application subsystem**
- Dual-core application subsystem 32 MHz operation
- 32- bit Firmware Processor (reserved for system use) executes:
 - Bluetooth upper stack
 - Profiles
 - House-keeping code
- 32- bit Developer Processor executes:
 - Developer applications

- 32 Mb flash memory
- On-chip caches per core enable optimized performance and power consumption Bluetooth subsystem
- Qualified to Bluetooth v5.2 specification including 2 Mbps Bluetooth Low Energy
- Single ended antenna connection with on-chip balun and Tx/Rx switch
- Bluetooth, Bluetooth Low Energy, and mixed topologies supported
- Class 1 support
- **Li-ion battery charger**
 - Integrated battery charger supporting up to 200 mA charge current
 - Variable float (or termination) voltage adjustable in 50 mV steps from 3.65 V to 4.4 V
 - Thermal monitoring and management are available in application software
 - Pre-charge to fast charge transition configurable at 2.5 V, 2.9 V, 3.0 V, and 3.1 V
- **Power management**
 - Integrated power management unit (PMU) to minimize external components
 - H340A runs directly from a Li-ion, USB, or external supply (2.8 V to 6.5 V)
 - Auto-switching between battery and USB (or other) charging source
 - Power islands employed to optimize power consumption for variety of use-cases
 - Dual switch-mode power supply (SMPS):
 - Automatic mode selection to minimize power consumption
 - 1.8 V SMPS generates power for both the device and off-chip circuits
 - Dedicated digital SMPS (output voltage changes automatically to minimize device power consumption)
- **Audio engine and digital audio interfaces**
 - 1 x unidirectional 24-bit inter-integrated circuit sound (I²S) interface
 - Mono analog output configurable as differential Class-AB earphone speaker output or differential high efficiency Class-D output:
 - Class-D signal-to-noise ratio (SNR): 99.3 dBA typ.
 - Class-D total harmonic distortion plus noise (THD +N): 93.5 dB typ.
 - Class-AB SNR: 100.9 dBA typ.
 - Class-AB THD+N: 93.5 dB typ.
 - Dual analog inputs configurable as single ended line inputs or, unbalanced or balanced analog microphone inputs:
 - SNR single-ended: 101.1 dBA typ.
 - THD+N single-ended: 85.9 dB typ.
 - 1 microphone bias (single bias shared by the two channels):
 - Crosstalk attenuation between two inputs using recommended application circuit: 80 dB typ.
 - Digital microphone inputs with capability to interface up to 8 digital microphones
 - Both analog-to-digital converter (ADC)s and the digital-toanalog converter (DAC) support sample rates of 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz. The DAC also supports 192 kHz and 384 kHz.
- **Peripherals and physical interfaces**
 - A universal asynchronous receiver transmitter (UART) interface
 - 2 x Bit Serializers (programmable serial peripheral interface (SPI) and inter-integrated circuit interface (I²C) hardware accelerator)
 - 1 x USB interface:
 - A full speed USB (USB-FS) Device (12 Mbps) – USB interface includes ESD protection to IEC-61000-4-2 (device level)
 - Internal NOR flash interface
 - Encryption to protect developer code and data

Encryption programmable with a 128-bit security key of original equipment manufacturer (OEM) choice stored in on-chip one-time programmable (OTP) memory

- Up to 22 programmable input/output (PIO) and 5 open drain/digital input light-emitting diode (LED) pads with pulse width modulation (PWM)

1.3 Application

- Wired/wireless stereo headsets/headphones
- Qualcomm TrueWireless™ stereo earbuds
- Wireless adapters and USB dongles
- Wireless adapters without /with OLED (for example: 1.3 inches, 0.96 inches).
- Wireless adapters with one stream or dual stream in TX Mode 、RX Mode 、TX and RX Mode.
- Wireless adapters with one stream or dual stream support aptX 、aptX LL 、aptX HD 、aptX adaptive 、SBC codecs.
- Support LINE IN and SPDIF

2 General Specification

Table1:

Feature	Specification
Chip	QCC3040BGA
Model	MY-BT302D
Dimensions	13mm(W) X 18mm(L) X 2.8mm(H)
Bluetooth Version	Bluetooth 5.2 Dual-Mode
Operating Voltage Range	VDD_BAT 2.8~4.6V (3.7V)
	VDD_CHG 4.7~6.5V (5.0V)
	VDD_IO 1.7~3.6V (1.8V)
	VDD_USB 2.8~3.5V (3.3V)
Charger Current	Internal 2~200mA
	External 200~1800mA
Frequency	2.402GHz -2.483GHz ISM band
LED Open drain current	50mA
Modulation	GFSK, $\pi/4$ -DQPSK, 8-DPSK
Antenna	External Antenna
Work Tem	-40°C to +85°C
Storage Tem	-40°C to +85°C
Humidity	10%~95% Non-Condensing
Environment	RoHS Compliant

2.1 Audio performance

Digital-to-analog converters

Class-D DAC audio output

Parameter	Conditions	Min	Typ	Max	Unit
Input Sample Width	-	-	-	24	Bits
Input Sample Rate, F_{sample}	-	8	-	192	kHz
Output Power	0 dBFS, 32 Ω load -3 dBFS, 16 Ω load	-	-	30	mW
Load	-	16	32	30k	Ω
SNR	$f_{\text{in}} = 1 \text{ kHz}$ 48 kHz F_{sample} B/W = 20 Hz \rightarrow 20 kHz A-Weighted 0 dBFS 32 Ω load	-	99.3	-	dBA
THD+N	$f_{\text{in}} = 1 \text{ kHz}$ 48 kHz B/W = 20 Hz \rightarrow 20 kHz -1 dBFS 32 Ω load	-	93.5	-	dB
Digital gain	Digital gain resolution = 1/32	-24.0	-	21.5	dB
Max capacitive load	Per terminal to ground	-	-	100	pF

Class-AB DAC audio output

Parameter	Conditions	Min	Typ	Max	Unit
Input Sample Width	-	-	-	24	Bits
Input Sample Rate, F_{sample}	-	8	-	192	kHz
Output Power	0 dBFS, 32 Ω load -3 dBFS, 16 Ω load	-	-	30	mW
Load	-	16	32	30k	Ω
SNR	$f_{\text{in}} = 1 \text{ kHz}$ 48 kHz F_{sample} B/W = 20 Hz \rightarrow 20 kHz A-Weighted 0 dBFS 32 Ω load	-	100.9	-	dBA
THD+N	$f_{\text{in}} = 1 \text{ kHz}$ 48 kHz B/W = 20 Hz \rightarrow 20 kHz -1 dBFS 32 Ω load	-	93.5	-	dB
Digital gain	Digital gain resolution = 1/32	-24.0	-	21.5	dB

Analog-to-digital converters

High-quality (HQADC) single-ended audio input

Parameter	Conditions	Min	Typ	Max	Unit
Output Sample Width	-	-	-	24	Bits
Output Sample Rate, F_{sample}	-	8	-	96	kHz
Input level	-	-	-	2.4	V pk-pk
Input impedance	0 dB to 24 dB analog gain	-	20	-	k Ω
	27 dB to 39 dB analog gain	-	10	-	k Ω
SNR	$f_{\text{in}} = 1 \text{ kHz}$ 48 kHz A-Weighted THD+N < 0.1% 2.4 V pk-pk input (0 dB gain)	-	101.1	-	dB
THD+N	$f_{\text{in}} = 1 \text{ kHz}$ 48 kHz 2.4 V pk-pk input (0 dB gain)	-	85.9	-	dB
Digital gain	Digital gain resolution = 1/32	-24.0	-	21.5	dB
Analog gain	3 dB steps	0	-	39	dB

High-quality (HQADC) differential audio input

Parameter	Conditions	Min	Typ	Max	Unit
Output Sample Width	-	-	-	24	Bits
Output Sample Rate, F_{sample}	-	8	-	96	kHz
Input level	-	-	-	2.4	V pk-pk
Input impedance	0 dB to 24 dB analog gain	-	20	-	k Ω
	27 dB to 39 dB analog gain	-	10	-	k Ω
SNR	$f_{\text{in}} = 1 \text{ kHz}$ 48 kHz A-Weighted THD+N < 0.1% 2.4 V pk-pk input (0 dB gain)	-	99.4	-	dB
THD+N	$f_{\text{in}} = 1 \text{ kHz}$ 48 kHz 2.4 V pk-pk input (0 dB gain)	-	95.5	-	dB
Digital gain	Digital gain resolution = 1/32	-24.0	-	21.5	dB
Analog gain	3 dB steps	0	-	39	dB

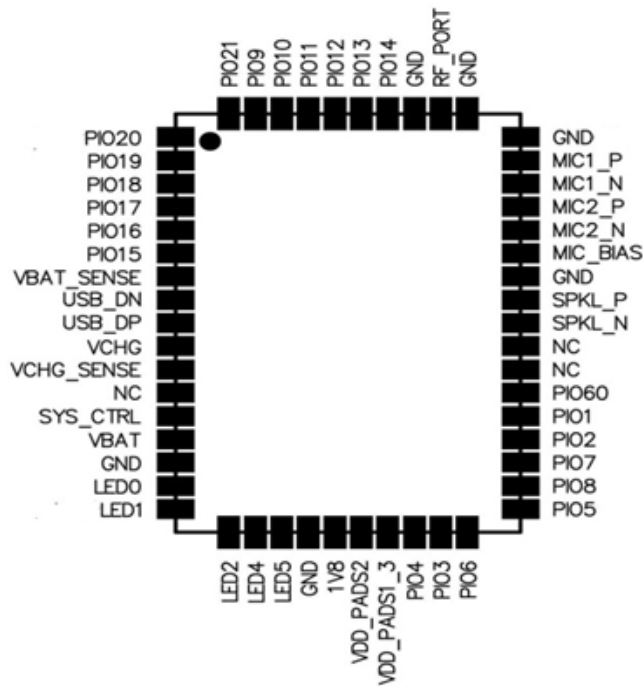
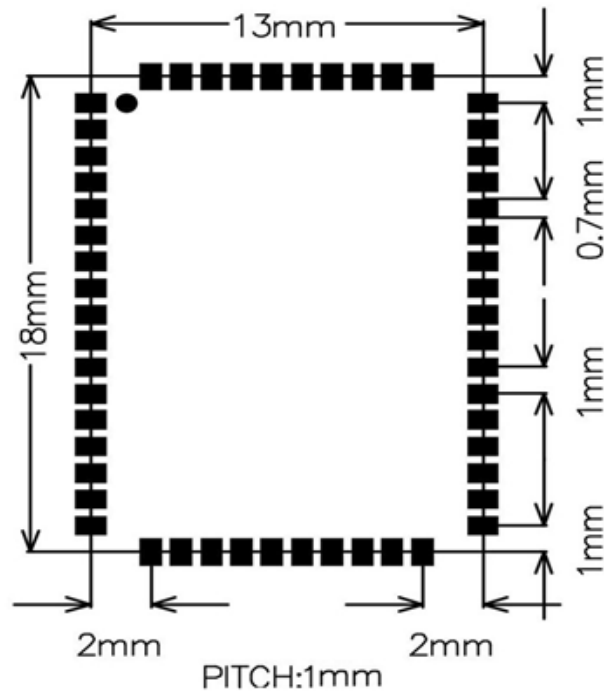
Microphone bias

Parameter	Conditions	Min	Typ	Max	Unit
Output voltage (Tunable, step = 0.1 V)	-	1.5	-	2.1	V
Output current capability	-	0.07	-	3.00	mA
Output noise	B/W = 20 Hz → 20 kHz Unweighted	4.5	5.1	7.3	μVrms
Crosstalk between microphones	Using recommended application circuit	-	80	-	dB
Load capacitance ^a	From parasitic PCB routing and package	-	-	0.1	nF

Shenzhen Muyu Technology Co., Ltd

3 Hardware Specification

3.1 Block Diagram and Pin Definition Diagram



3.2 PIN Definition Descriptions

Table2:

Pin	Pin Name	Type	PIN Descriptions
1	PIO[20]	I/O	Programmable input/ output line
2	PIO[19]	I/O	Programmable input/ output line
3	PIO[18]	I/O	Programmable input/ output line
4	PIO[17]	I/O	Programmable input/ output line
5	PIO[16]	I/O	Programmable input/ output line
6	PIO[15]	I/O	Programmable input/ output line
7	VBAT_SENSE	Analog	Battery voltage sense input
8	USB DN	Digital	USB Full Speed device D- I/O IEC-61000-4-2 (device level) ESD Protection
9	USB DP	Digital	USB Full Speed device D+ I/O IEC-61000-4-2 (device level) ESD Protection
10	VCHG	Supply	Charger input to Bypass regulator Charger input sense pin after external mode sense-resistor. High impedance NOTE If using internal charger or no charger, connect VCHG_SENSE direct to VCHG
11	VCHG_SENSE	Analog	Charger input sense pin. High impedance. Connect VCHG_SENSE direct to SMPS_VCHG
12	NC	NC	NC
13	SYS CTRL	Digital input	Typically connected to an ON/OFF push button. If power is present from the battery and/or charger, and software has placed the device in the OFF or DORMANT state, a button press boots the device. Also usable as a digital input in normal operation. No pull. Additional function: PIO[0] input only
14	VBAT	Supply	Battery voltage input
15	GND	Ground	Ground
16	AIO[0] / LED[0]	Analog or digital input/ open drain output	General-purpose analog/digital input or open drain LED output
17	AIO[1]/LED[1]	Analog or digital input/ open drain output	General-purpose analog/digital input or open drain LED output
18	AIO[2]/LED[2]	Analog or digital input/ open drain output	General-purpose analog/digital input or open drain LED output

19	AIO[4]/LED[4]	Analog or digital input/ open drain output	General-purpose analog/digital input or open drain LED output
20	AIO[5]/LED[5]	Analog or digital input/ open drain output	General-purpose analog/digital input or open drain LED output
21	GND	Ground	Ground
22	1V8	Supply	18V voltage output
23	VDD PADS 2	Supply	18 V/3 3 V PIO supply
24	VDD PADS1 3	Supply	18 V/3 3 V PIO supply
25	PIO[4]	I/O	Programmable input/ output line Alternative function : TBR_MOSI[1]
26	PIO[3]	I/O	Programmable input/ output line Alternative function : TBR_MISO[2]
27	PIO[6]	I/O	Programmable input/ output line Alternative function : TBR_MOSI[0]
28	PIO[5]	I/O	Programmable input/ output line Alternative function : TBR_MOSI[1]
29	PIO[8]	I/O	Programmable input/ output line Alternative function : TBR CLK
30	PIO[7]	I/O	Programmable input/ output line Alternative function : TBR_MISO[0]
31	PIO[2]	I/O	Programmable input/ output line Alternative function : TBR_MISO[3]
32	PIO[1]	I/O	Automatically defaults to RESET# mode when the device is unpowered, or in off modes. Reconfigurable as a PIO after boot. Alternative function: Programmable I/O line 1
33	PIO[60]	I/O	Programmable input/ output line
34	NC	NC	NC
35	NC	NC	NC
36	AUDIO HPL_N / SPKL_N	Analog	Headphone/speaker differential left output, negative Alternative function: Differential left line output, negative
37	AUDIO HPL_P / SPKL_P	Analog	Headphone/speaker differential left output, positive Alternative function Differential left line output, positive
38	GND	Ground	Ground
39	AUDIO MIC BIAS	Analog	Mic bias output
40	AUDIO MIC2_N / LINEIN R_N	Analog	Microphone differential 2 input, negative Alternative function: Differential audio line input right, negative
41	AUDIO MIC2_P / LINEIN R_P	Analog	Microphone differential 2 input, positive. Alternative function: Differential audio line input right,

			positive
42	AUDIO MIC1 N/ LINEIN L_N	Analog	Microphone differential 1 input, negative. Alternative function: Differential audio line input left, negative
43	AUDIO MIC1_P / LINEIN L_P	Analog	Microphone differential 1 input, positive. Alternative function: Differential audio line input left, positive
44	GND	Ground	Ground
45	GND	Ground	Ground
46	BT RF	RF	Bluetooth transmit/receive
47	GND	Ground	Ground
48	PIO[14]	I/O	Digital Bidirectional with programmable strength internal pull- up/pull-down Digital Bidirectional with programmable strength internal
49	PIO[13]	I/O	pull- up/pull-down
50	PIO[12]	I/O	Programmable input/ output line
51	PIO[11]	I/O	Programmable input/ output line
52	PIO[10]	I/O	Programmable input/ output line
53	PIO[9]	I/O	Programmable input/ output line
54	PIO[21]	I/O	Programmable input/ output line

4 Physical Interface

4.1 UART interface

MY-BT302D has a standard UART serial interface that provides a simple mechanism to communicate with other serial devices using the RS232 protocol. The UART interface multiplexes with PIOs and other functions. Hardware flow control is optional. Table lists possible UART settings.

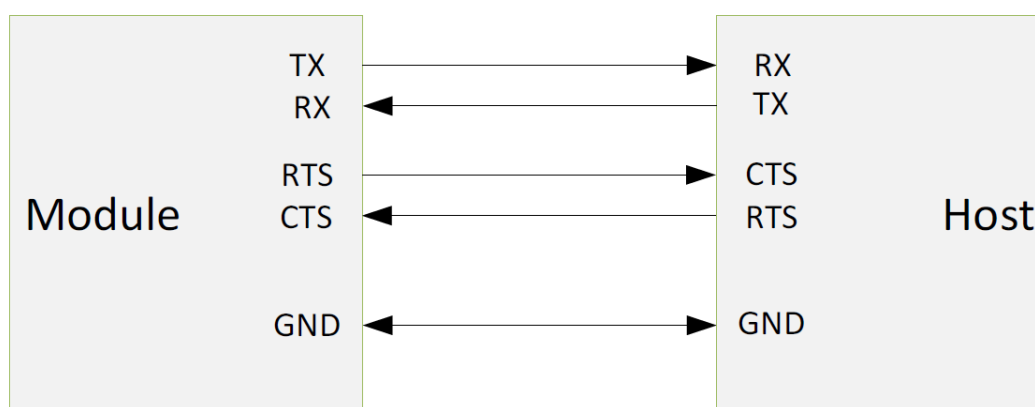
UART configuration options

Parameter		Possible value
Baud rate	Minimum	2400 Bd ($\leq 2\%$ Error)
		19,200 Bd ($\leq 1\%$ Error)
	Maximum	4 MBd ($\leq 1\%$ Error)
Flow control		RTS/CTS or None
Parity		None, Odd, or Even
Number of stop bits		1 or 2
Bits per byte		8

Standard UART baud rates

lists common baud rates and the H340A percentage error for that rate.

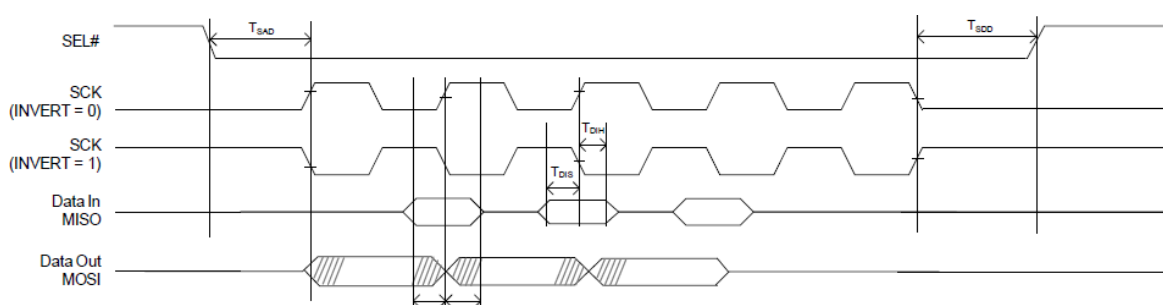
Baud rate	Error (%)
1200	18.62
2400	-1.73
4800	-1.73
9600	-1.73
19200	0.82
38400	-0.45
57600	-0.03
76800	0.18
115200	-0.03
230400	-0.03
460800	-0.03
921600	0.02
1382400	0.01
1843200	0.00
2764800	0.01
3686400	0.00
4000000	0.00



UART Connection

4.2 SPI master

Figure shows and Table lists bitserial interface timings.



Bitserial M-SPI timing diagram

Bitserial M-SPI timing parameters

Parameter	Symbol	Min	Max	Unit	Notes
Sel assert to SCK rise delay	T_{SAD}	17.0	-	ns	-
SCK fall to SEL de-assert delay	T_{SDD}	52.5	-	ns	-
MISO data setup	T_{DIS}	39.3	-	ns	Added to slave device access time. Total must be < T(SCK)
MISO data hold	T_{DIH}	0.0	-	ns	-
MOSI data invalid minimum	T_{DV1}	-13.0	-	ns	Total data invalid window of 28.1 ns
MOSI data invalid maximum	T_{DV2}	-	15.1	ns	

NOTE When operating in this mode the SCK has a maximum frequency of 16 MHz.

4.3 I²C master

MY-BT302D is compliant with the Fast-mode UM10204 I²C -bus specification.

5 Electrical Characteristics

5.1 Battery input pin specification

Battery specifications common to all regulators

VBAT	Min	Typ	Max	Unit
Operating voltage	2.8	3.7	4.6	V
Software power-off threshold	-	3	-	V
Under voltage lockout rising threshold	2.47	2.60	2.73	V
Under voltage lockout hysteresis	50	-	120	mV
USB dead/weak battery rising threshold	3.14	3.30	3.46	V
USB dead/weak battery hysteresis	50	-	120	mV

5.2 Charger input pin specification

VCHG specifications common to all regulators

VCHG	Min	Typ	Max	Unit
Operating voltage (full charger specification)	4.75	5.00	6.50	V
Operating voltage (reduced charger specification)	4.00	5.00	6.50	V
VCHG_PRESENT rising threshold	3.4	3.6	4.0	V
VCHG_PRESENT hysteresis	70	-	150	mV
Full operating range	VCHG_PRESENT	-	6.5	V
On chip pull-down (disabled when VCHG_PRESENT = 1)	10	20	30	kΩ

5.3 Digital terminals

Digital terminals	Min	Typ	Max	Unit
VDD_PADS supply	1.7	1.8	3.6	V
VIL input logic level low	-	-	0.22 x VDD_PADS	V
VIH input logic level high	0.7 x VDD_PADS	-	-	V
Drive current (configurable)	2, 4, 8, 12	4	-	mA
VOL output logic level low, at max rated drive	-	-	0.22 x VDD_PADS	V
VOH output logic level high, at max rated drive	0.75 x VDD_PADS	-	-	V
Strong pull (up and down)	15	65	150	kΩ
Weak pull (up and down)	500	2200	5000	kΩ

5.4 LED driver pads

LED driver pads		Min	Typ	Max	Unit
Open drain current	High impedance state	-	-	5	μA
	Current sink state	-	-	50	mA
LED pad resistance	V < 0.5 V	-	-	12	Ω
VIL input logic level low		-	-	0.4	V
VIH input logic level high		1.0	-	-	V

5.5 VBAT voltage measurement accuracy

Measurement	Min	Typ	Max	Unit
VBAT_SENSE voltage measurement accuracy	-	± 1	± 3	%

5.6 Absolute Maximum Ratings

Rating	Minimum	Maximum
Storage temperature	-40°C	+85°C

5.7 Recommended Operating Conditions

Operating Condition	Minimum	Maximum
Operating temperature range	-40°C	+85°C
Supply voltage: VBAT	+2.8V	+4.3V

6 ESD & MSL

Table 6:

Parameter	Value
MSL:	Grade: 3
ESD:	HBM: Class-2 CDM: Class-B

7 Recommended Temperature Reflow Profile

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccant (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the Picture below and follow instructions specified by IPC/JEDEC J-STD-033.

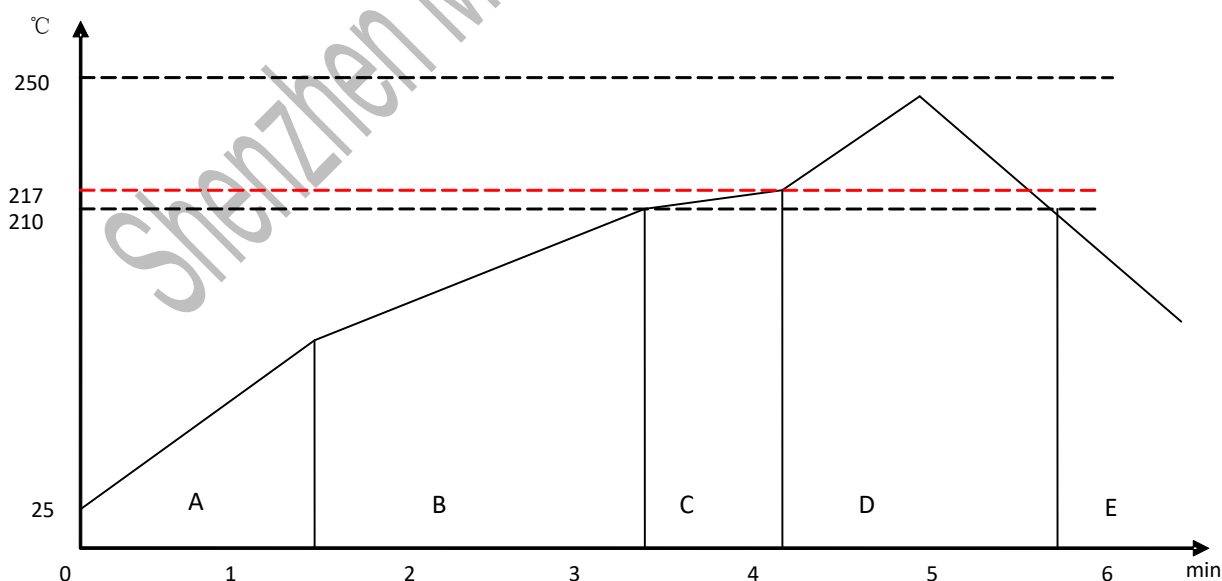
Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the Picture below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccant and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH

Table 7: Recommended baking times and temperatures

MSL	125°C Baking Temp		90°C/≤ 5%RH Baking Temp		40°C/ ≤ 5%RH Baking Temp	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours@ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours@ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72hours@ 30°C/60%
3	9 hours	7 hours	33hours	23 hours	13 days	9 days

The design of the surface mount module is easy to manufacture, including reflow soldering to the PCB motherboard. Ultimately, it is the customer's responsibility to choose a suitable solder paste and ensure that the furnace temperature during reflow meets the requirements of the solder paste. The surface mount module complies with the J-STD-020D1 standard for reflow soldering temperature. The welding profile depends on the various parameters that need to be set for each application. The data here is only for the guidance of reflow soldering.



Typical Lead-free-flow

Preheating zone (A)-This zone heats up at a controlled rate, with a typical value of 0.5-2°C/s. The purpose of this area is to preheat the PCB board and components to 120~150°C. At this stage, the heat needs to be evenly distributed to the PCB board, and the solvent is completely removed to reduce the thermal shock of the components.

Equilibrium Zone 1 (B)-At this stage, the flux becomes soft and evenly encapsulates the solder particles and spreads them on the PCB board to prevent them from being re-oxidized. As the temperature rises and the flux is liquefied, each activator and rosin are activated and begin to eliminate the oxide film formed on the surface of each solder particle and PCB board. For this area, the recommended temperature is 150° to 210°, and the time is 60 to 120 seconds.

Equilibrium zone 2 (C) (optional)-In order to solve the problem of upright parts, it is recommended to keep the temperature at 210-217°C for about 20 to 30 seconds.

Reflow zone (D)-The curve in the figure is designed for Sn / Ag3.0 / Cu0.5. It can be a reference for other lead-free solders. The peak temperature should be high enough to achieve good wettability, but not too high to cause discoloration or damage to the component. Excessive welding time will lead to intermetallic growth, leading to brittle solder joints. The recommended peak temperature (Tp) is 230~250°C. When the temperature is higher than 217°C, the welding time should be 30 to 90 seconds.

Cooling zone (E)-The cooling rate should be fast to keep the solder particles small, which will provide a longer lasting solder joint. The typical cooling rate should be 4°C.

8 Mechanical Detail

8.1 Physical Dimensions

- Dimension: 13mm(W) x 27mm(L) x 2.2 mm(H) Tolerance: ±0.2mm
- Pad size: 1.6mmX0.6mm Tolerance: ±0.1mm
- Pad pitch: 1.0mm Tolerance: ±0.1mm

9 Hardware Integration Suggestions

9.1 Soldering Recommendations

MY-BT302D is compatible with the industry standard reflow profile of lead-free solder. The reflow profile used depends on the thermal quality of the entire assembled PCB, the heat transfer efficiency of the oven, and the specific type of solder paste used. Please refer to the data sheet of the specific solder paste for the profile configuration.

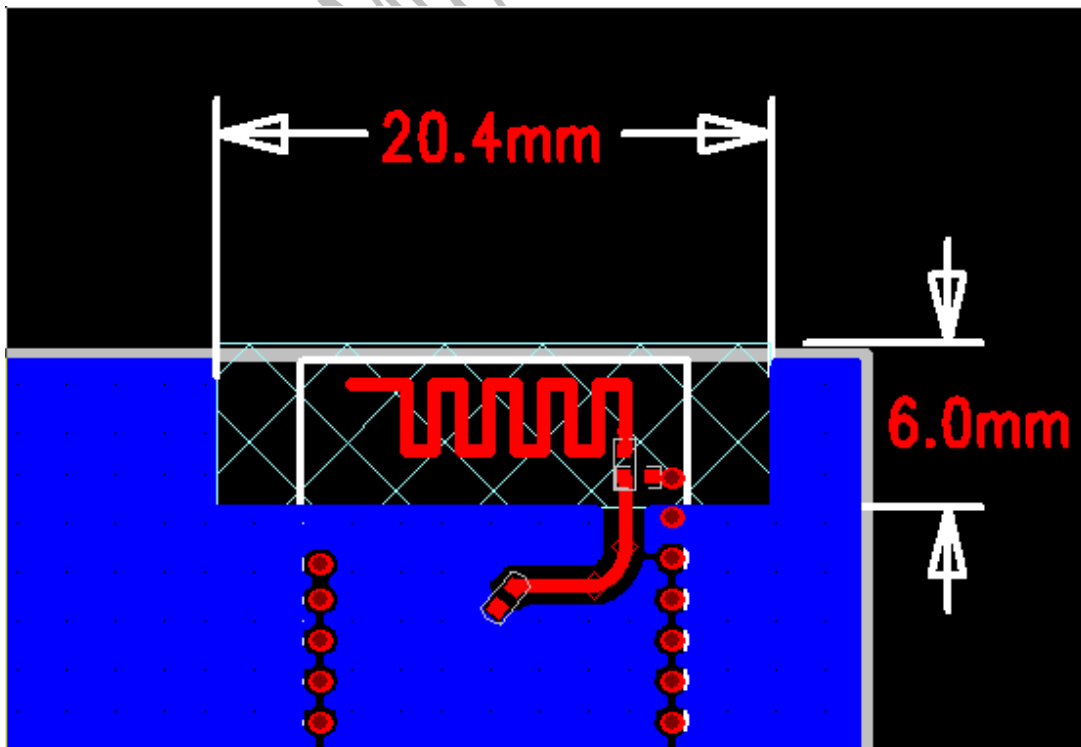
Muyu will provide the following suggestions for welding modules to ensure the reliability of the solder joints and operations of the modules after welding. Since the reflow profile used is dependent on the process and layout, the best reflow profile should be studied on a case-by-case basis. Therefore, the following recommendations should be used as a starting point.

9.2 Layout Guidelines (Internal Antenna)

It is strongly recommended to use good layout practices to ensure the normal operation of the module. Placing copper or any metal close to the antenna will affect the performance of the antenna, thereby deteriorating the working efficiency of the antenna. The metal shield around the antenna will prevent signal radiation, so the metal casing should not be used with the module. Please use more grounding vias at the edge of the grounding area.

The following suggestions can help avoid EMC problems in the design. Please note that each design is unique, and the following description does not consider all basic design rules, such as avoiding capacitive coupling between signal lines. The following description aims to avoid EMC problems caused by the RF part of the module. Please consider carefully to avoid problems with the digital signal in the design.

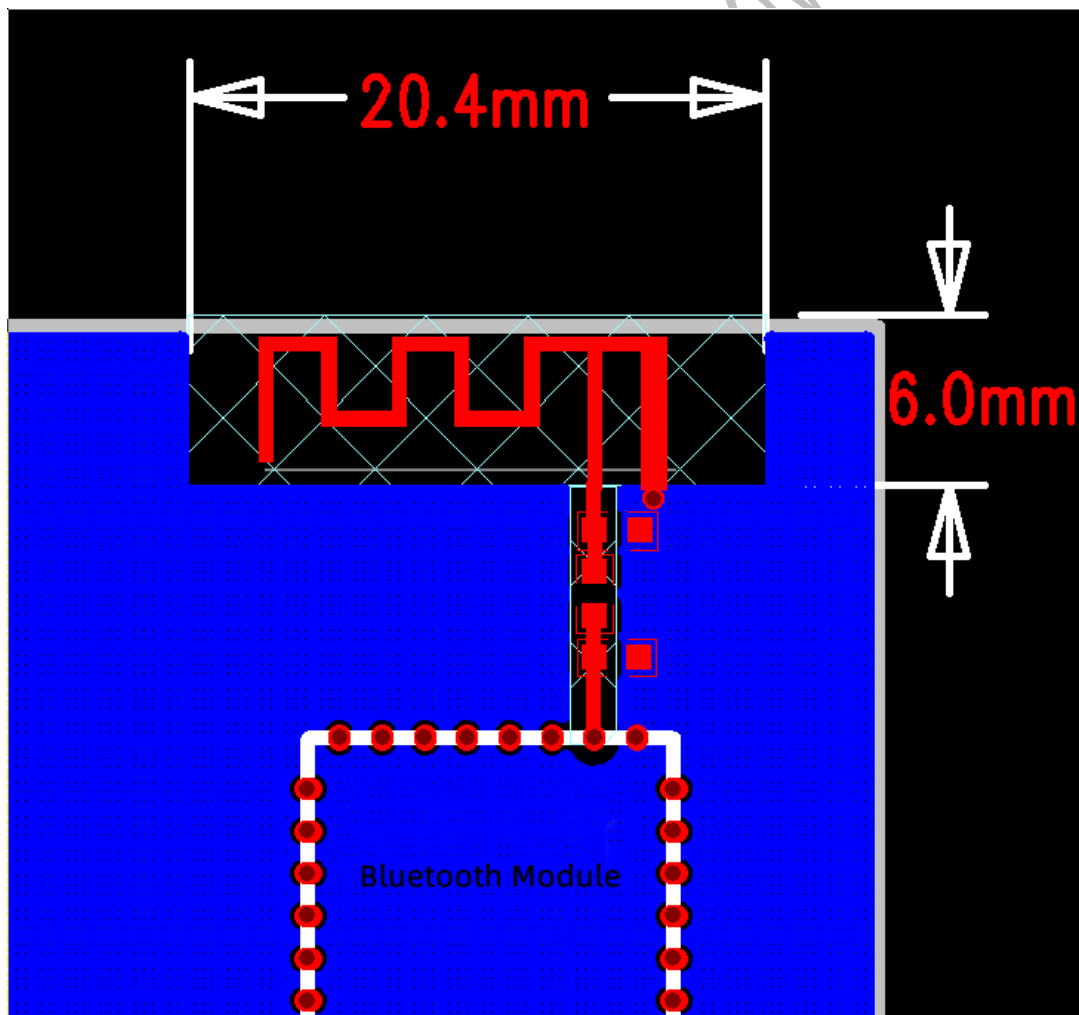
Make sure that the loop of the signal wire is as short as possible. For example, if the signal enters the inner layer through vias, always use ground vias around the pad. And place them closely and symmetrically around the signal vias. Any sensitive signal traces and loops should be completed on the inner layer of the PCB as much as possible. Sensitive signal lines should have an area surrounded by ground wires above and below. If this is not possible, make sure that the return path is shortest (for example, use the ground wire next to the signal wire)



9.3 Layout Guidelines (External Antenna)

In the absence of on-board antenna design, module placement and PCB layout are critical to optimizing module RF performance.

1. The microstrip line (the wiring from the antenna to the EXT_ANT port on the module end) should be 50Ω ;
2. The microstrip line should be as straight as possible and as short as possible. When it is necessary to turn, it should be as arc as possible;
3. The width of the microstrip line is about 0.5mm, and the distance between the copper coating and the microstrip line is about 0.5mm;
4. To avoid interference to the module signal; the location of the external antenna and the EXT_ANT port of the module should be far away from any noise sources and digital lines, the antenna should be placed close to the board, no components and copper should be placed around, and no wiring should be placed as far as possible, Keep it intact;
5. A Π -type matching network circuit is needed between the microstrip lines, and placed as close to the antenna as possible to better match the impedance;
6. The RF key circuit of the module should be clearly separated from any digital circuit on the system board



9.4 General Design Suggestions

Wireless products are not suitable for the use of external metal casings and large metal components around them. The length of PCB traces or wires should be as short as possible.

The distance between the connection on the top layer and the ground area should be at least as large as the thickness of the dielectric.

Avoid placing RF close to the digital part of the system board.

In order to reduce signal loss, avoid wiring the microstrip line in sharp corners. Chamfered or rounded wiring is preferred to rectangular wiring; 45-degree oblique wiring is better than pure 90-degree wiring.

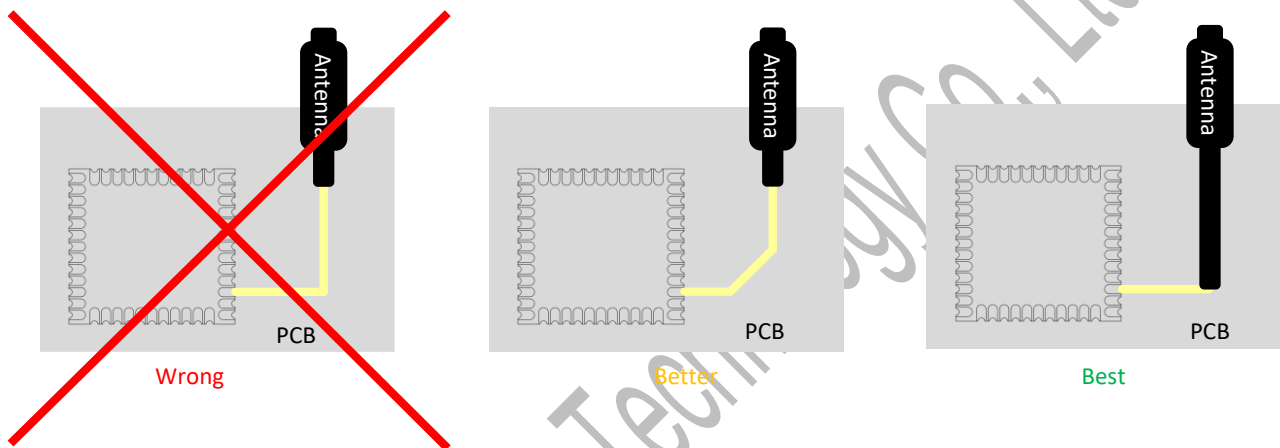


Figure 11: Recommended Trace Connects Antenna and the Module

Avoid placing RF connections on the other side of the module. The distance from the microstrip line to the ground plane at the bottom of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled. Use as many vias as possible to connect the ground planes.

10 Product Packaging Information

- Pallet packaging
- Pallet size: 180mm * 195mm
- 50pcs/Pallet
- MOQ: 1000pcs



11 Application Schematic

